REMARKS

Present Status of the Application

The Office Action rejected claims 1-8, under 35 U.S.C. 103(a), as being unpatentable over Chakravorty (US 6,181,569) in view of Chao (US 5,622,899). The Office Action rejected claims 10, 15-18 and 20, under 35 U.S.C. 103(a), as being unpatentable over Chakravorty (US 6,181,569) in view of Chao (US 5,622,899).

Applicant has amended claim 1 to more clearly define the present invention. The limitation added in claim 1 is described in [0026] and shown in Fig. 2C, and thus no new matter is entered. Claims 1-8, 10, 15-18 and 20 remain pending in the present invention, and reconsideration of those claims is respectfully requested.

Claim Rejections under 35 U.S.C. 103(a)

The Office Action rejected claims 1-8, under 35 U.S.C. 103(a), as being unpatentable over Chakravorty (US 6,181,569) in view of Chao (US 5,622,899). Applicant respectfully traverses the 103(a) rejection of claims 1-8 because the two references combined do not teach each and every element recited in these claims.

The present invention is related to a stress relieving method as amended claim 1 recites:

Claim 1. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that at least no circuits are formed on the dielectric layer within the first area;

forming a plurality of first openings in the dielectric layer within the first area; and

forming a first material layer over the wafer, wherein ***the upper surface of the first material layer has pits at locations directly over the first openings***, and the first material layer is a high stress dielectric layer.

The office action interprets the reference 308 in Fig. 5 of the Chakravorty reference as the first material layer of claim 1. However, in the layer 308, the opening 309 ***is not located directly over*** the opening (above 304). In claim 1 of the present application, the upper surface of the first material layer has ***pits at locations directly over the first openings*** formed in the dielectric layer within the first area.

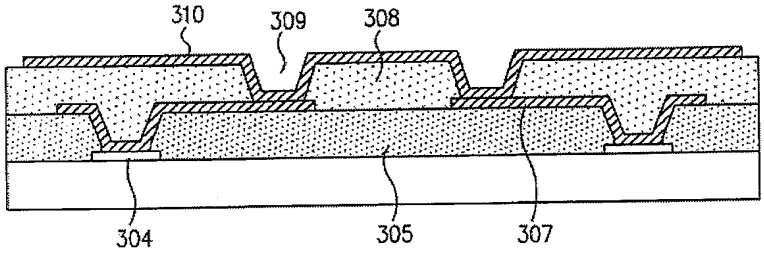

FIG. 5

In view of the foregoing or other reasons, Applicant respectfully submits independent claim 1 patently defines over Chakravorty and Chao, and should be allowed. Since independent

claim 1 should be allowed over the prior art of record, its dependent claims 2-8 should also be allowed as a matter of law, because the dependent claims contain all features of their respective independent claim 1.

In particular, regarding to claims 2 and 5, the office action interprets the reference 303 in Fig. 6 of the Chakravorty reference as the scribe line. But, as a matter of fact, Fig. 6 is one of the steps for a chip package process, and **the structure shown in Fig. 6 is in the region where the chip 302 is disposed**. That is, Fig. 6 does not show any scribe line. Please see Fig. 2 and col. 7, lines 45-47, Chakravorty disclosed the reference number 302 refers as a chip while **the reference number 303 refers as a scribe line IN FIG. 2**. The step shown in Fig. 6 is followed Figs. 4-5a, and the chip contact pads are labeled as reference number 304, and **obviously, the chip contact pads in Fig. 6 is mis-labeled as reference number 303**. Therefore, Fig. 6 of the citation does not show the scribe line.

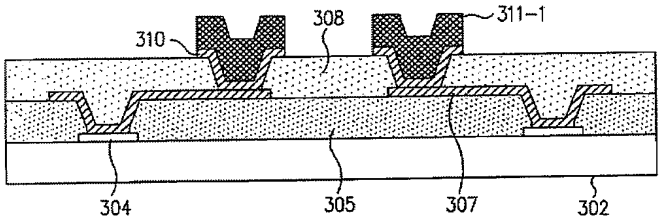

FIG. 5a

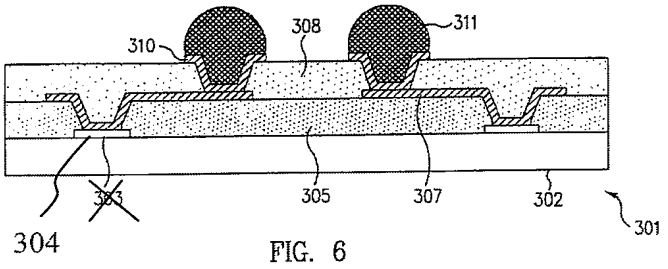

FIG. 6

The Office Action rejected claims 10, 15-18 and 20, under 35 U.S.C. 103(a), as being unpatentable over Chakravorty (US 6,181,569) in view of Chao (US 5,622,899). Applicant respectfully traverses the 103(a) rejection of claims 10, 15-18 and 20 because the two references combined do not teach each and every element recited in these claims.

The present invention is related to a stress relieving method as claim 10 recites:

Claim 10. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that no circuits are formed within the first area, ***the first area comprising a scribe line, the second area comprising a region for forming a die, wherein there is no opening formed in the dielectric layer within the first area***;

forming a first material layer over the wafer to cover the dielectric layer; and

forming a plurality of first openings in the first material layer within the first area. (Emphasis added)

The office action stated Chakravorty does not teach "the first area comprising a scribe line, the second area comprising a region for forming a die, wherein there is no opening formed in the dielectric layer within the first area", but Chao disclosed the feature in Fig. 2A-2B. In particular, the office action interprets the reference 21 as the scribe line and the reference 22 as a region for the die. However, as a matter of fact, Chao teaches **the reference 21 is a semiconductor chip** and **the reference 22 is used as a scribe line** (see col. 3, lines 39-45). Chao fails to teach no circuits are formed within the first area (scribe line 22), there is no opening formed in the dielectric layer within the first area (scribe line 22) and forming a plurality of first openings in the first material layer within the first area (scribe line 22).

In view of the foregoing or other reasons, Applicant respectfully submits Chakravorty and Chao fail to teach or suggest every element recited in claim 10. Therefore, Applicant respectfully submits that independent claim 10 patently defines over the prior art references, and should be allowed. Since independent claim 10 should be allowed over the prior art of record, its dependent claims 15-18 and 20 should also be allowed as a matter of law, because the dependent claims contain all features of their respective independent claim 10.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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